REMARKS

Claims 1-10 and 12-20 are pending herein. Claims 7-10, 15 and 16 are withdrawn.

By this Amendment, claim 1 is amended to incorporate the original subject matter of claims 3 and 4. Claims 3 and 4 are amended to more fully distinguish the invention of the claims from the reference cited against the claims, and claims 3-7 and 12-14 are amended. Claim 11 is canceled, and claims 17-20 are added.

No new matter is added by this Amendment. Support for the amendments to the claims is found in the original specification and claims. In particular, support for the language added to claim 1 is found in original claims 3 and 4. Support for the language added to claims 3 and 4 is found at, for example, page 4, lines 15-17 of the present specification. Support for new claims 17-19 are found in original claim 6 and support for new claim 20 is found in original claim 1, as well as at, for example, page 4, lines 15-17 of the present specification.

I. Rejoinder

Applicant notes with appreciation that the Patent Office has indicated that upon allowance of the elected product claims, the non-elected process claims will be considered for rejoinder.

In accordance with MPEP §821.04, if product claims are elected and subsequently allowed, rejoinder of non-elected process claims which depend from or otherwise include all of the limitations of allowed product claims will be permitted.

Accordingly, upon allowance of elected claims 1-6, 12-14 and 17-20, non-elected claims 7-10, 15 and 16 should be rejoined and similarly allowed.

II. Claim Objections

Claims 1-6 and 11-14 were objected to because in claim 1 the term "one layer" should allegedly read as "one of the two layers" and because in claims 3 and 11 the term "two layers" should allegedly read as "the two layers."

Claim 1 is herein amended as suggested by the Examiner. Withdrawn claim 7 is similarly amended.

Claim 3 is herein amended and the objection with respect to claim 3 is no longer relevant and therefore moot.

Claim 11 is herein canceled, thus the objection with respect to claim 11 is moot.

For the foregoing reasons, Applicant respectfully submits that the objections have been overcome. Reconsideration and withdrawal of the objections are thus respectfully requested.

III. Rejection Under 35 U.S.C. §102(b)

Claims 1-5 and 11-14 were rejected under 35 U.S.C. §102(b) as allegedly being anticipated by U.S. Patent No. 3,754,214 (hereinafter "Matsumoto"). This rejection is respectfully traversed.

Claim 11 is herein canceled. Thus, with respect to claim 11, this rejection is moot.

Claims 2-5 and 12-14 depend, directly or indirectly, from claim 1.

Claim 1 recites a memory device comprising a memory element including a layer of piezoelectric material and a layer of ferroelectric material, the two layers being separated by a common electrode and an input electrode being provided on one of the two layers and an output electrode being provided on the other of the two layers, the input and output electrodes being disposed on opposite sides of their respective layers compared with the common electrode, the two layers being clamped together such as to enhance the amplitude of a voltage generated across one of the two layers due to the application of a voltage to the other

two layers. The memory device further comprises a comparator having a pair of inputs, the inputs being connected to the input and output electrodes, respectively, of the memory element, and an output for providing an indication of a logic state of the memory device.

Matsumoto describes an electronic security system (i.e., a "key-lock" type system) employing a pair of "adaptive memory devices" 24, 26 (see Figs 1 and 2 of Matsumoto). The device 24 acts as a key and is carried by a user. Device 26 acts as the "lock" and is associated with a comparator 30, the output of which, after amplification in an amplifier 21, operates an electro-mechanical latch 14, presumably to open a door, or the like. The two memory devices are connected via a three-way connector, which joins lines 16-16', 18-18' and 20-20'.

Further, each memory device 24, 26, as shown in Fig. 2 of Matsumoto, consists of a pair of ferroelectric layers 42, 44 separated by an electrode 50. The outer faces of the ferroelectric layers 42, 44 are coated with respective electrodes 46 and 48. The layers 42, 44 form a pair of equivalent capacitors 38, 40, as shown in Figure 3 of Matsumoto. Two additional components include an oscillator 28 and a "pulse charging unit" 34. The oscillator places an oscillating signal on one of the two outer electrodes, namely electrode 46, while the pulse charging unit 34 places a voltage on the other outer electrode, namely electrode 48.

It appears that in the operation of the security system, the polarization of the memory devices is set by applying one or more pulses from the pulse charging unit 34, shown in Fig. 4 of Matsumoto, between terminals 2 and 3 and terminals 2' and 3' of the devices 24 and 26, respectively. Depending on the amplitude, length and number of the pulses, the layer 44 can be set to have a maximum (saturation) polarization in either of two opposite directions, or any desired degree of polarization in between. (See col. 4, line 63 to col. 5, line 9 and col. 5, line 33 to col. 6, line 2 of Matsumoto). Such setting of the polarization matches the "key" memory device 24 to the "lock" memory device 26, so that when the user connects the "key" to the "lock," the comparator will be switched over and operate the latch 14.

After the "setting" procedure, the "key" can be connected to the "lock" and the oscillator 28 will then presumably place an "input" alternating signal across the layer 42 in both memory devices. (Although the oscillator is shown as connected to the terminal 1 on the electrode 46, it appears that the oscillator signal may be applied between the terminals 1 and 3, especially since terminals 3 and 3' are called "common terminals" in col. 2, lines 34-36.)

The apparent application of this alternating voltage across layer 42 in the two memory devices becomes transformed into mechanical energy, which is passed on to the layer 44 in the two devices, which then performs the opposite transformation, namely back to electrical energy. In this way, a difference in voltage is formed between the terminals 2 and 2', which is sensed in the comparator 30. If the "key" and "lock" both "fit," that is, were set to the same initial polarization, then the latch 14 will be operated.

However, Matsumoto fails to disclose that the two layers 42, 44 in each memory device are "clamped together." It appears that the Patent Office is assuming that the layers are clamped together because the devices function as a transformer. However, such a device will have some transforming effect even without deliberate clamping, though the effect will be comparatively slight. By contrast, in the present invention, clamping is deliberately carried out in order to enhance the transforming effect. That is, clamping the two layers together is required by claim 1.

Matsumoto further fails to disclose a memory device. Whereas claim 1 recites a memory device and a memory element and a comparator output which is for providing an indication of the logic state of the memory device. Thus, references to a memory function exist not only in the preamble of claim 1, but also in the body.

Further, the comparator 30 of Matsumoto is not connected to the input and output electrodes (that is, terminals 1 and 2) of one of the memory devices 24, 26 as recited in claim 1. Instead, Matsumoto teaches that the comparator 30 is connected to the output terminals of

the two memory devices. This highlights a fundamental difference between the present invention and that disclosed in Matsumoto. In Matsumoto, the adaptive memory devices are employed in a differential configuration, whereas in the present application one or more memory devices are used in isolation as individual memories. In Matsumoto, the comparator appears to compare the phases of the signals across the "output" layers 44 only of the memory devices. By contrast, in the present invention, the comparator compares the phase of the signal across one of the two layers with the phase of the signal across the other of the two layers.

For the foregoing reasons, Applicant submits that Matsumoto fails to anticipate or render obvious the subject matter of claim 1. That is, nowhere does Matsumoto teach or suggest a memory device comprising a memory element including a layer of piezoelectric material and a layer of ferroelectric material, the two layers being separated by a common electrode and an input electrode being provided on one of the two layers and an output electrode being provided on the other of the two layers, the input and output electrodes being disposed on opposite sides of their respective layers compared with the common electrode, the two layers being clamped together such as to enhance the amplitude of a voltage generated across one of the two layers due to the application of a voltage to the other two layers, and a comparator having a pair of inputs, the inputs being connected to the input and output electrodes, respectively, of the memory element, as recited in claim 1.

Further, nowhere does Matsumoto teach or suggest a memory device wherein the two layers are clamped together by one of a means for maintaining a constant spacing between the input and output electrodes, and a means for exerting a constant force or stress upon one of the input and output electrodes relative to the other of the input and output electrodes, as recited in claims 3, 4 and 20.

For the foregoing reasons, Applicant submits that Matsumoto fails to anticipate or render obvious the subject matter of claims 1 and 20, or the claims dependent therefrom. Reconsideration and withdrawal of the rejection are thus respectfully requested.

IV. Rejection Under 35 U.S.C. §103(a)

Claim 6 was rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Matsumoto in view of U.S. Patent No. 5,060,191 (hereinafter "Nagasaki"). This rejection is respectfully traversed.

The Patent Office acknowledges that Matsumoto does not expressly disclose that the input and output electrodes are parallel with each other and perpendicular to the common electrode. However, the Patent Office refers to the stripe electrodes 3 and 5 in Fig. 1 of Nagasaki when alleging that one of ordinary skill in the art would have readily recognized that in a memory device, the relevant electrodes are commonly formed perpendicular to each other in order to form an addressable high memory capacitance matrix structure.

However, Fig. 1 of Nagasaki appears to show an orthogonal configuration of the two arrays of electrodes for a single ferroelectric layer 3. Figures 4 and 6 of Nagasaki show a laminated configuration of the array shown in Fig. 1. Here, each lamination layer has its own orthogonal array of electrodes 3 and 5.

Moreover, neither Matsumoto nor Nagasaki teach or suggest an array of "common electrodes" orthogonal to both of the outer electrode arrays, as required by claim 6.

For the foregoing reasons, Applicant submits that Matsumoto and Nagasaki, whether alone or in combination, fail to render obvious the subject matter of claim 6 or the claims dependent therefrom. Reconsideration and withdrawal of the rejection are thus respectfully requested.

V. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-10 and 12-20 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

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